FIG. 1

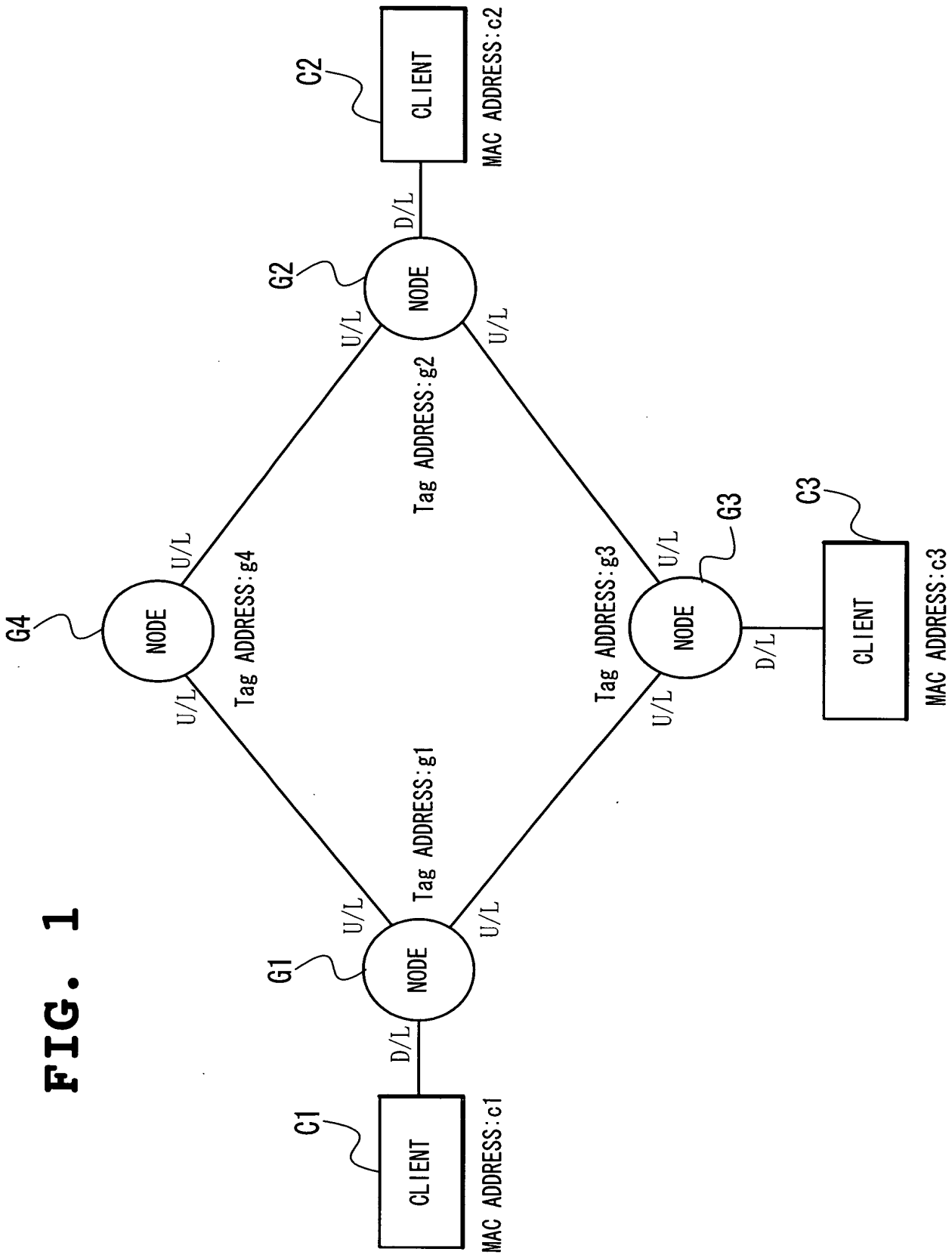

G4
NODE
U/L
U/L
Tag ADDRESS:g4
G2
NODE
U/L
U/L
Tag ADDRESS:g2
G1
NODE
U/L
U/L
Tag ADDRESS:g1
G3
NODE
U/L
U/L
Tag ADDRESS:g3
C2
CLIENT
MAC ADDRESS:c2
D/L
C1
CLIENT
MAC ADDRESS:c1
D/L
C3
CLIENT
MAC ADDRESS:c3
D/L

FIG 2

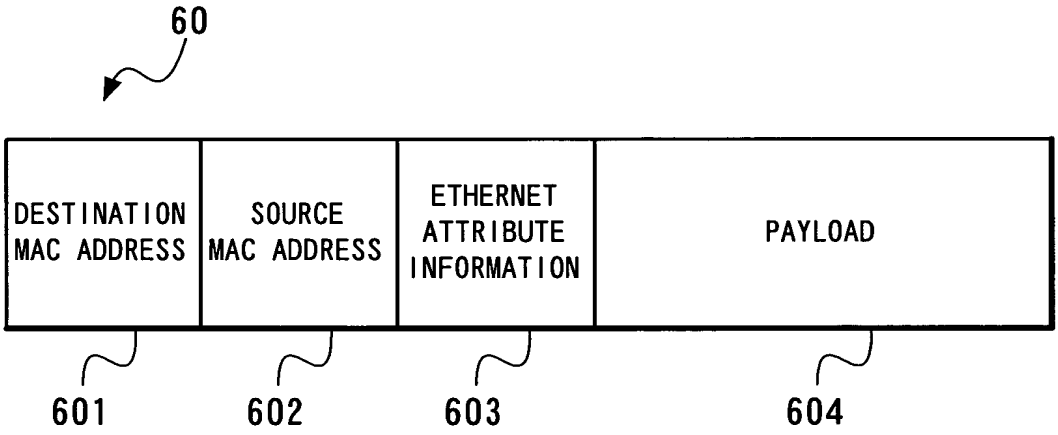


FIG. 3

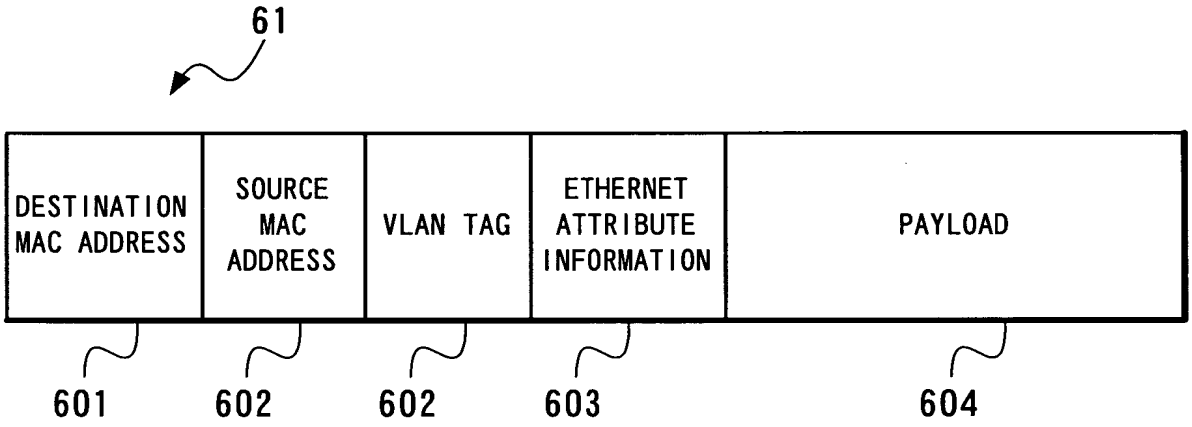


FIG. 4

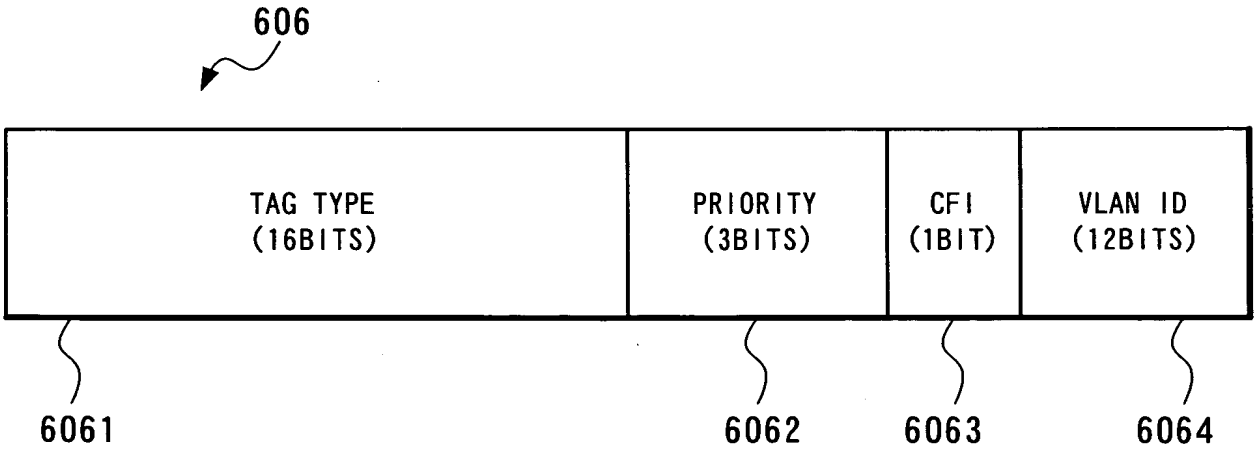


FIG. 5

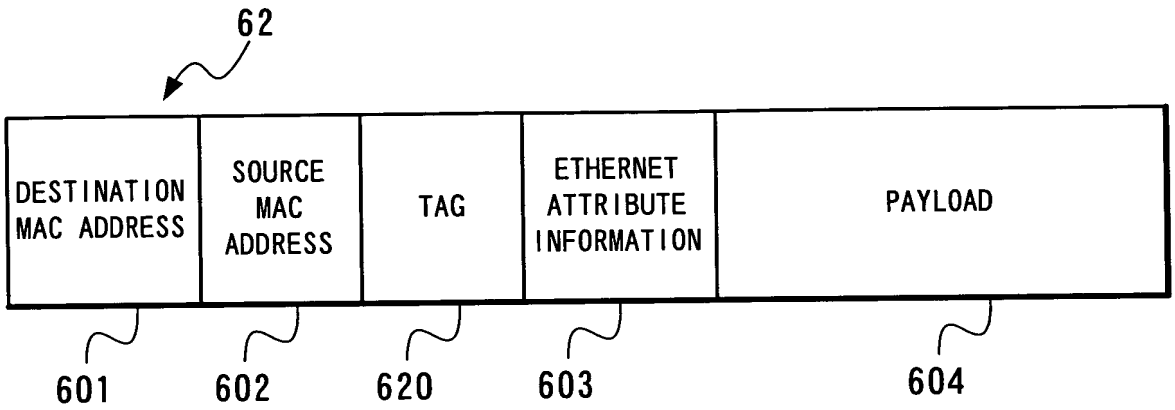


FIG. 6

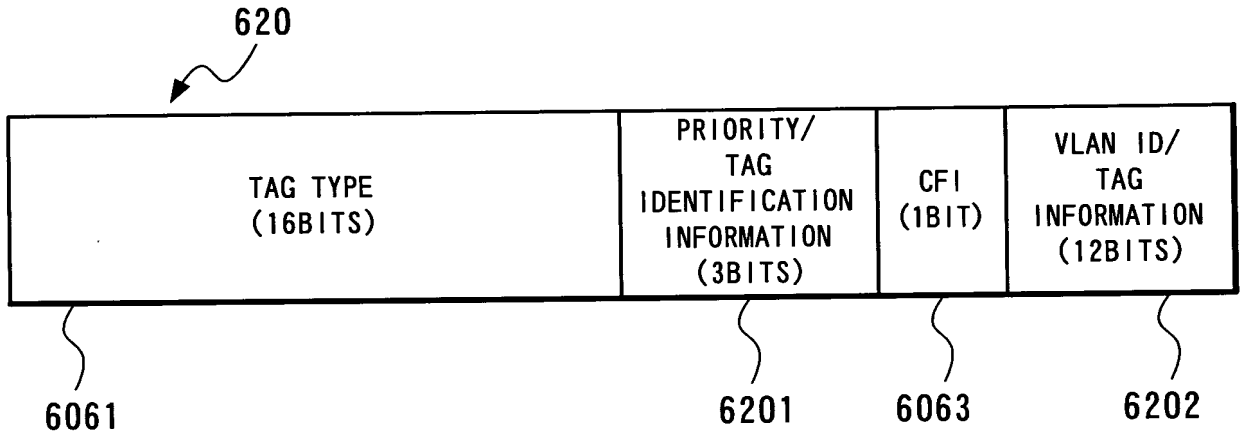


FIG. 7

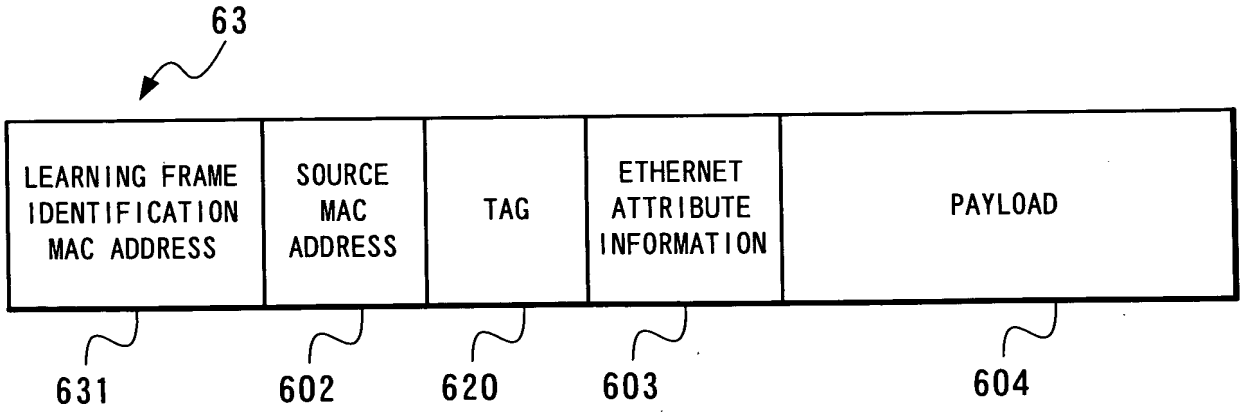


FIG. 8

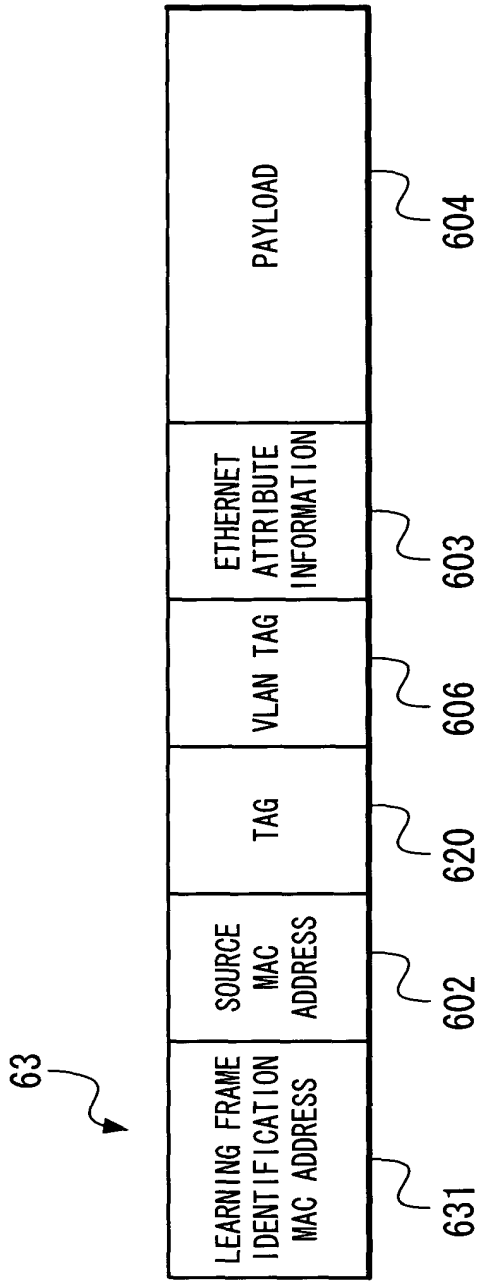

63
LEARNING FRAME IDENTIFICATION MAC ADDRESS
SOURCE MAC ADDRESS
TAG
VLAN TAG
ETHERNET ATTRIBUTE INFORMATION
PAYLOAD
631
602
620
606
603
604

FIG. 9

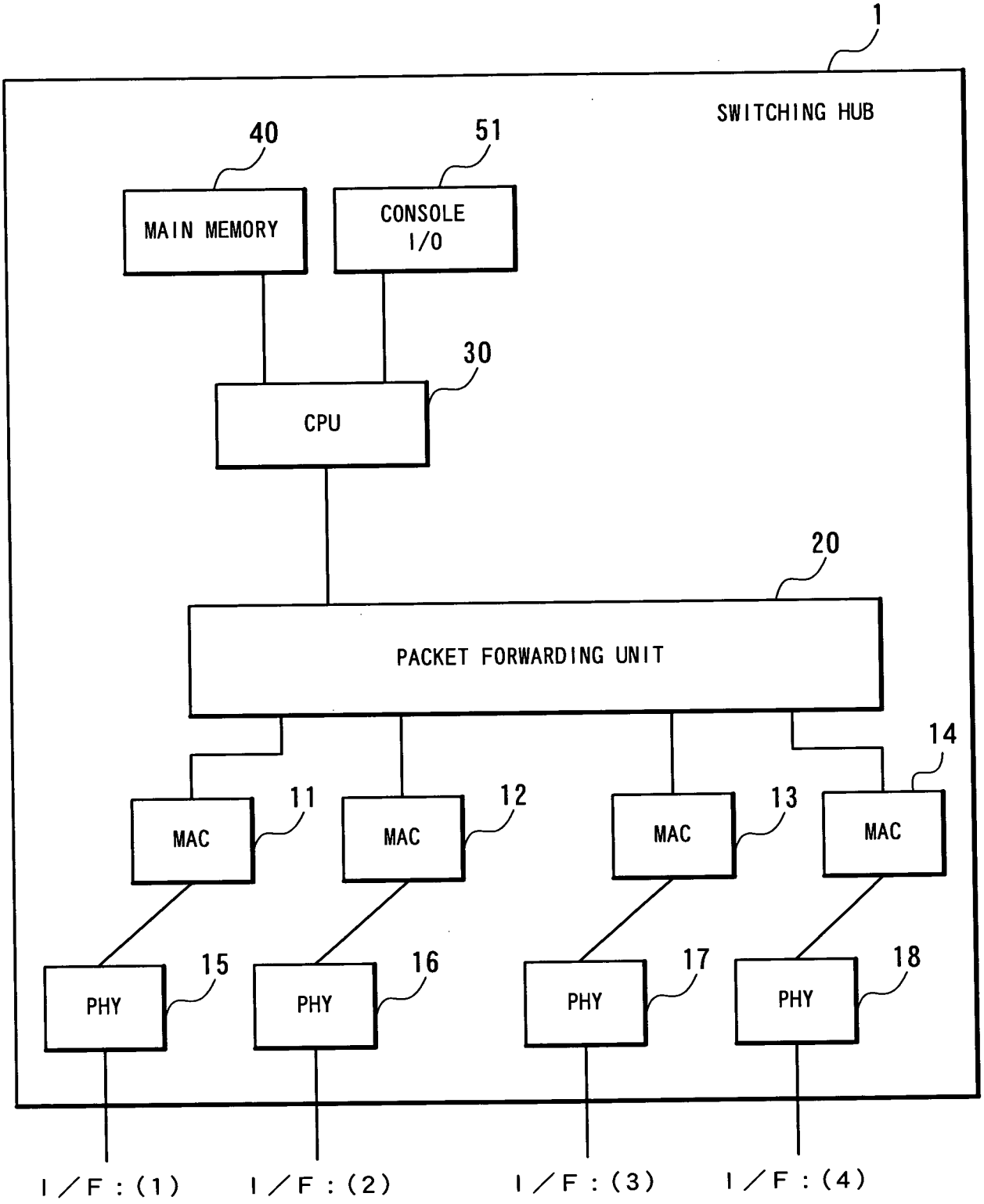

1
SWITCHING HUB
40
MAIN MEMORY
51
CONSOLE I/O
30
CPU
20
PACKET FORWARDING UNIT
14
MAC
11
MAC
12
MAC
13
MAC
PHY
15
PHY
16
PHY
17
PHY
18
I/F:(1)
I/F:(2)
I/F:(3)
I/F:(4)

FIG.10

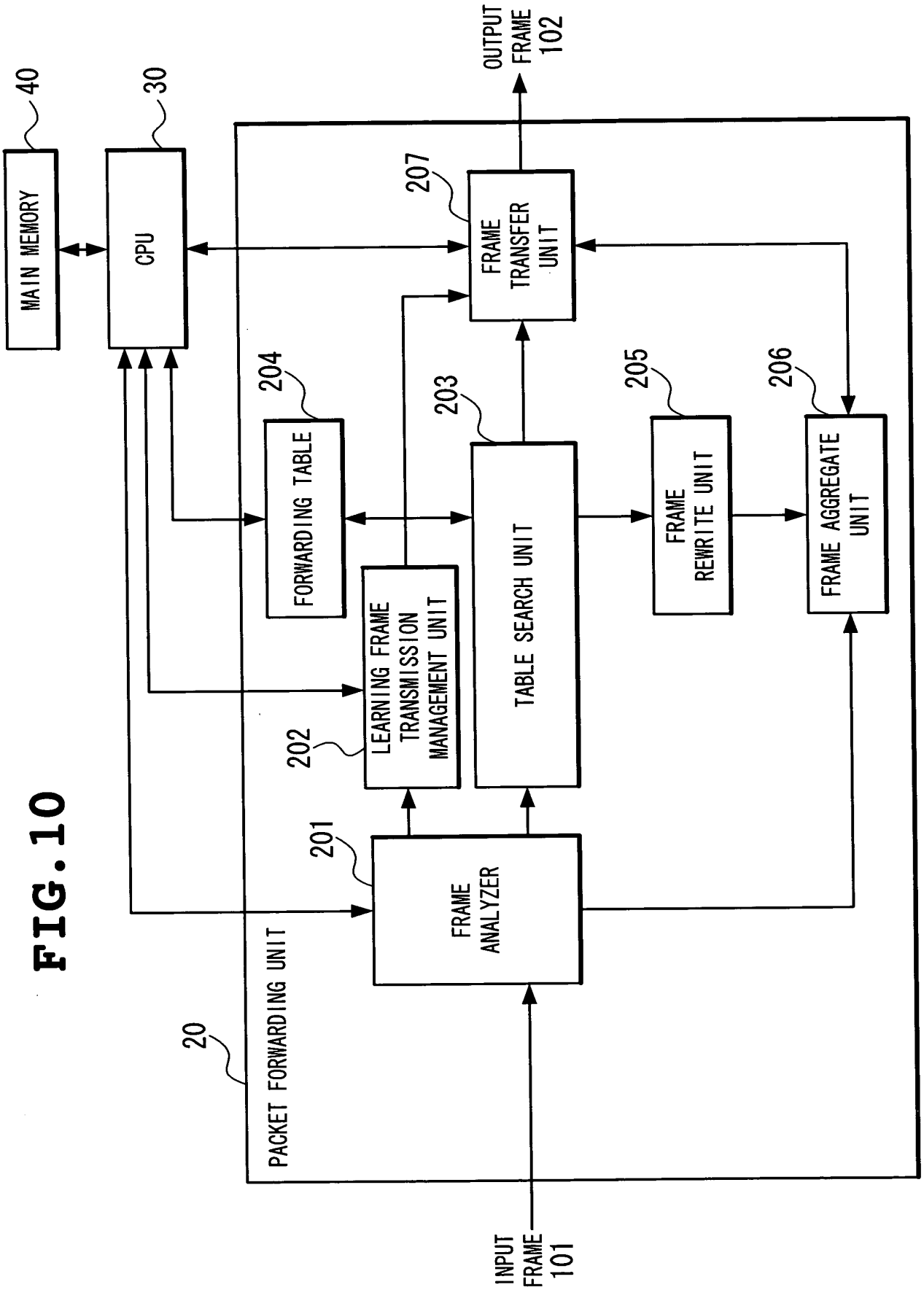

MAIN MEMORY
40
CPU
30
OUTPUT FRAME 102
207
FRAME TRANSFER UNIT
204
FORWARDING TABLE
203
TABLE SEARCH UNIT
205
FRAME REWRITE UNIT
206
FRAME AGGREGATE UNIT
LEARNING FRAME TRANSMISSION MANAGEMENT UNIT
202
201
FRAME ANALYZER
20
PACKET FORWARDING UNIT
INPUT FRAME 101

FIG. 11

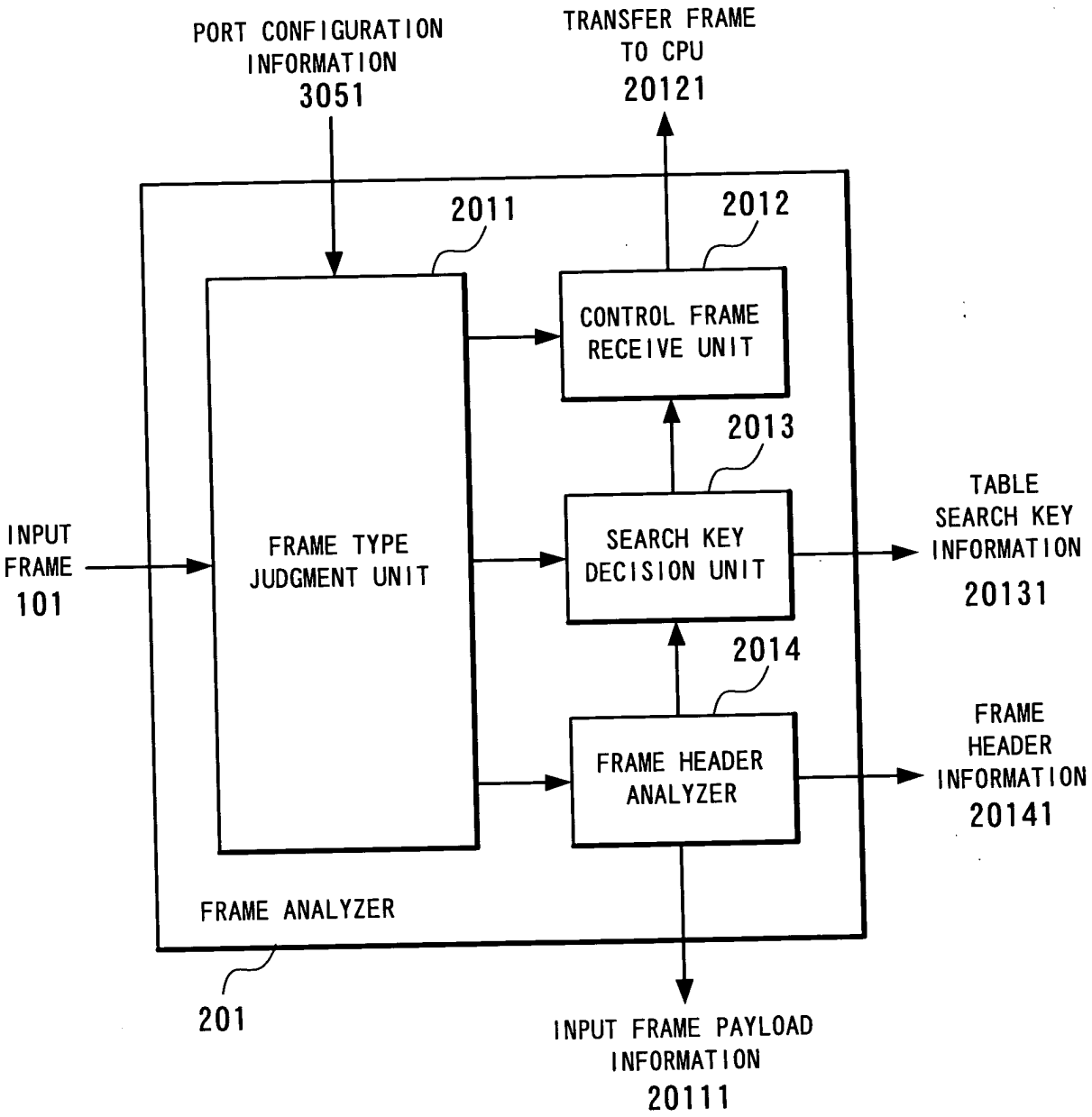

PORT CONFIGURATION INFORMATION
3051
TRANSFER FRAME TO CPU
20121
2011
2012
CONTROL FRAME RECEIVE UNIT
2013
INPUT FRAME
101
FRAME TYPE JUDGMENT UNIT
SEARCH KEY DECISION UNIT
TABLE SEARCH KEY INFORMATION
20131
2014
FRAME HEADER ANALYZER
FRAME HEADER INFORMATION
20141
FRAME ANALYZER
201
INPUT FRAME PAYLOAD INFORMATION
20111

FIG.12

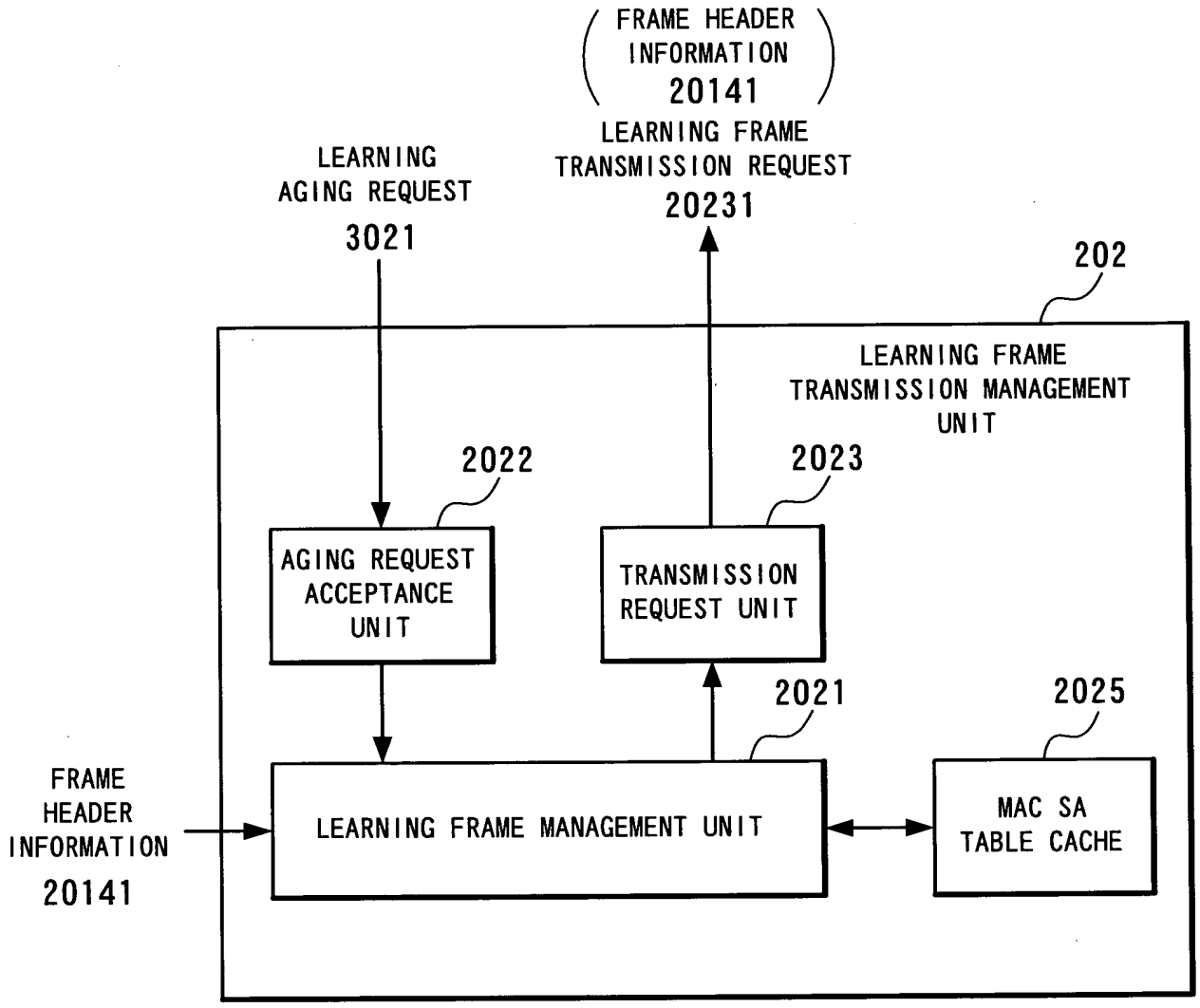

FRAME HEADER INFORMATION 20141
LEARNING FRAME TRANSMISSION REQUEST 20231
LEARNING AGING REQUEST 3021
202
LEARNING FRAME TRANSMISSION MANAGEMENT UNIT
2022
2023
AGING REQUEST ACCEPTANCE UNIT
TRANSMISSION REQUEST UNIT
2021
2025
FRAME HEADER INFORMATION 20141
LEARNING FRAME MANAGEMENT UNIT
MAC SA TABLE CACHE

FIG.13

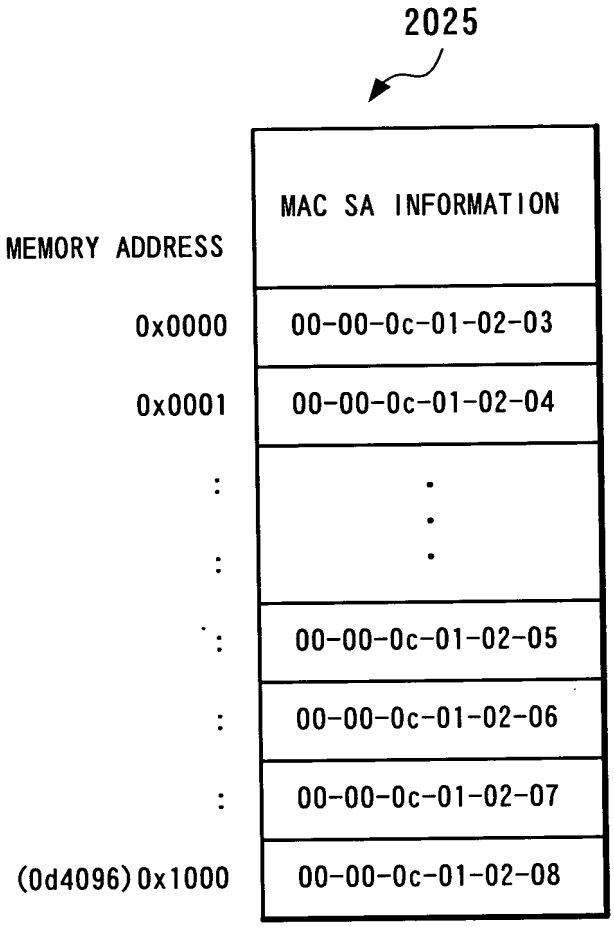

2025
MAC SA INFORMATION
MEMORY ADDRESS
0x0000
00-00-0c-01-02-03
0x0001
00-00-0c-01-02-04
:
:
:
:
00-00-0c-01-02-05
:
00-00-0c-01-02-06
:
00-00-0c-01-02-07
(0d4096)0x1000
00-00-0c-01-02-08

FIG.14

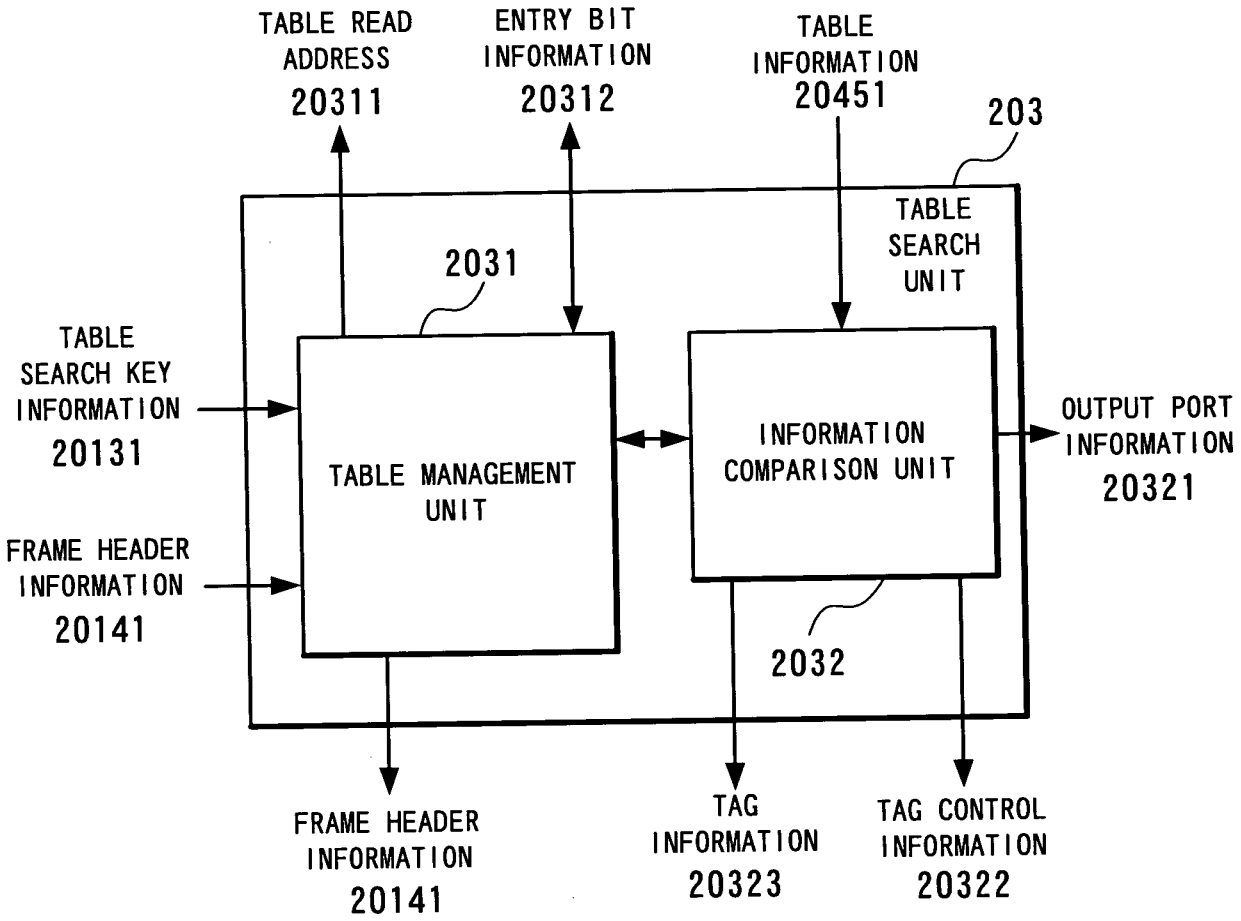


TABLE READ ADDRESS
20311
ENTRY BIT INFORMATION
20312
TABLE INFORMATION
20451
203
TABLE SEARCH UNIT
2031
TABLE SEARCH KEY INFORMATION
20131
FRAME HEADER INFORMATION
20141
TABLE MANAGEMENT UNIT
INFORMATION COMPARISON UNIT
OUTPUT PORT INFORMATION
20321
2032
FRAME HEADER INFORMATION
20141
TAG INFORMATION
20323
TAG CONTROL INFORMATION
20322

FIG.15

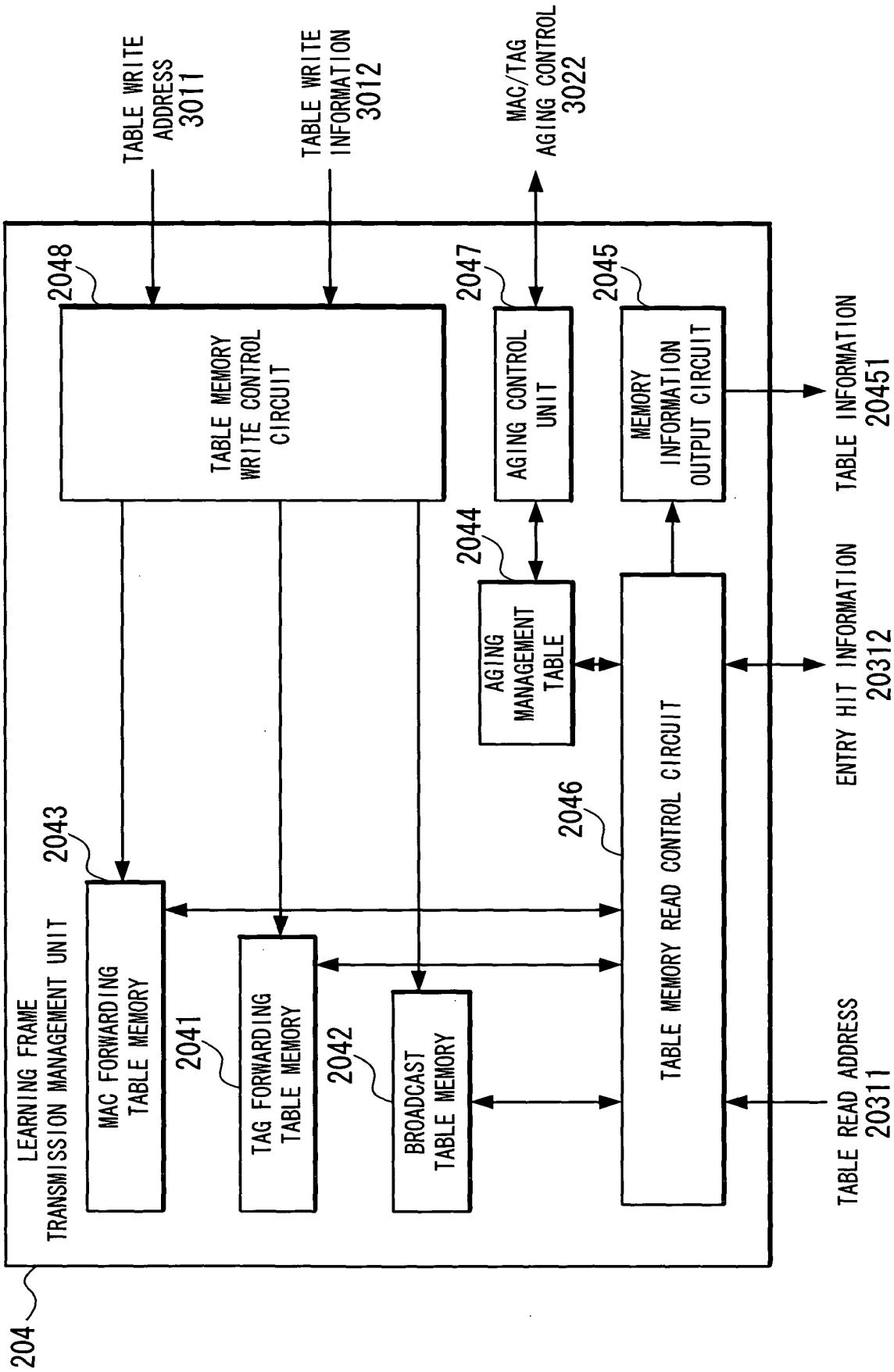


TABLE WRITE ADDRESS 3011
TABLE WRITE INFORMATION 3012
MAC/TAG AGING CONTROL 3022
2048
TABLE MEMORY WRITE CONTROL CIRCUIT
2047
AGING CONTROL UNIT
2045
MEMORY INFORMATION OUTPUT CIRCUIT
TABLE INFORMATION 20451
2044
AGING MANAGEMENT TABLE
2046
TABLE MEMORY READ CONTROL CIRCUIT
ENTRY HIT INFORMATION 20312
2043
MAC FORWARDING TABLE MEMORY
2041
TAG FORWARDING TABLE MEMORY
2042
BROADCAST TABLE MEMORY
LEARNING FRAME TRANSMISSION MANAGEMENT UNIT
TABLE READ ADDRESS 20311
204

FIG.16

2043

MEMORY ADDRESS	MAC DESTINATION ADDRESS (48BITS)	DESTINATION FIRST-STAGE TAG INFORMATION (32BITS)	ENTRY TYPE	OUTPUT PORT INFORMATION	FAULT TIME OUTPUT PORT INFORMATION	TAG CONTROL INFORMATION	(32BITS)
0x0000	00-00-0c-01-02-03	8100-0000	MAC→Tag	1	4	TAG INSERTION	8100-0001
0x0001	00-00-0c-01-02-04	8100-0000	MAC→Tag	1	4	TAG INSERTION	8100-0002
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
⋮	00-00-0c-01-02-05	8100-0000	MAC→PORT	2	3	NO TAG OPERATION	0000-0000
⋮	00-00-0c-01-02-06	8100-4000	MAC→PORT	3	0	NO TAG OPERATION	0000-0000
⋮	00-00-0c-01-02-07	8100-4000	MAC→PORT	3	0	NO TAG OPERATION	0000-0000
(0d8388706)0x7FFFFF	00-00-0c-01-02-08	8100-4000	MAC→PORT	1	4	NO TAG OPERATION	0000-0000

FIG.17

2041

MEMORY ADDRESS	OUTPUT PORT INFORMATION	FAULT TIME OUTPUT PORT INFORMATION
0x0000	1	4
0x0001	1	4
:	⋮	⋮
:		
:	2	3
:	3	0
:	3	0
(0d4096)0x1000	1	4

FIG.18

2042

MEMORY ADDRESS	PLURAL OUTPUT PORT INFORMATION
0x0000	1, 2
0x0001	1, 2
:	⋮
:	
:	2, 3
:	3
:	3
(0d4096)0x1000	1, 2

FIG.19

2044

MEMORY ADDRESS	MAC-TAG ENTRY MANAGEMENT INFORMATION	MAC-PORT ENTRY MANAGEMENT INFORMATION
0x0000	NO HIT	NO HIT
0x0001	HIT	HIT
:	.	.
:	.	.
:	ENTRY INVALID	ENTRY INVALID
:	ENTRY PROTECT	ENTRY PROTECT
:	NO HIT	NO HIT
(0d8388706)0x7FFFFF	HIT	HIT

FIG.20

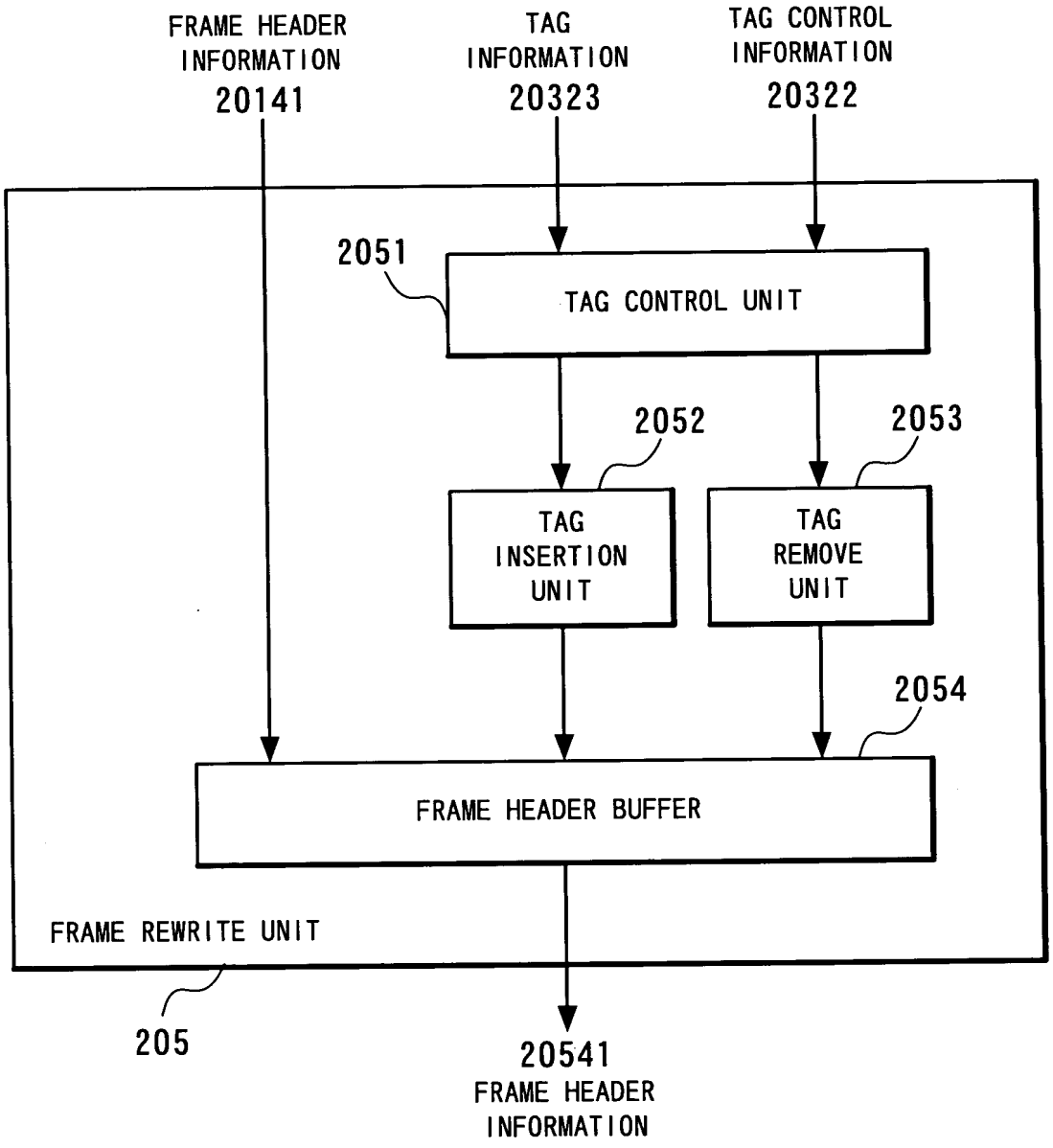

FRAME HEADER INFORMATION
20141
TAG INFORMATION
20323
TAG CONTROL INFORMATION
20322
2051
TAG CONTROL UNIT
2052
2053
TAG INSERTION UNIT
TAG REMOVE UNIT
2054
FRAME HEADER BUFFER
FRAME REWRITE UNIT
205
20541
FRAME HEADER INFORMATION

FIG.21

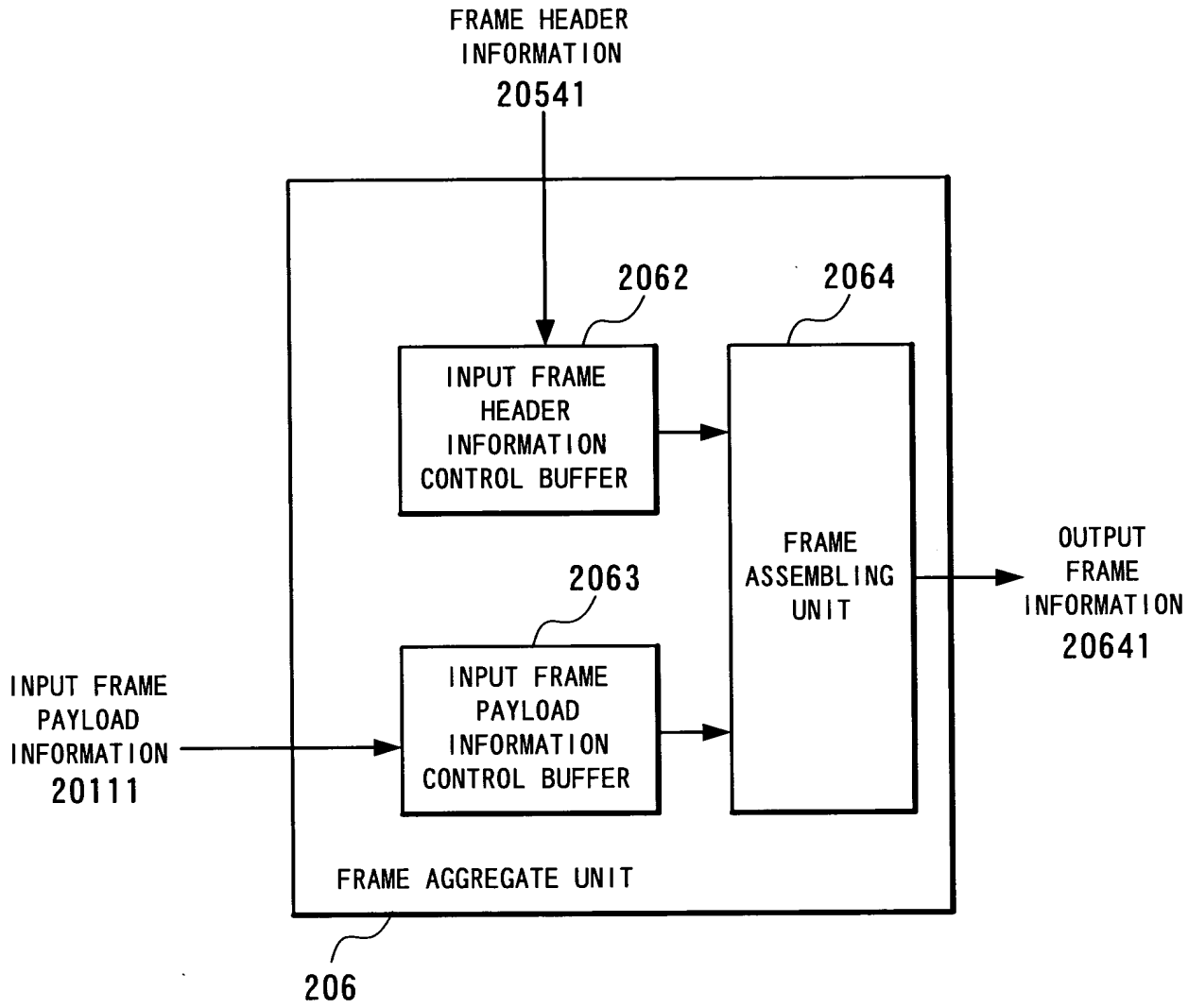

FRAME HEADER
INFORMATION
20541
2062
2064
INPUT FRAME
HEADER
INFORMATION
CONTROL BUFFER
FRAME
ASSEMBLING
UNIT
OUTPUT
FRAME
INFORMATION
20641
2063
INPUT FRAME
PAYLOAD
INFORMATION
20111
INPUT FRAME
PAYLOAD
INFORMATION
CONTROL BUFFER
FRAME AGGREGATE UNIT
206

FIG 22

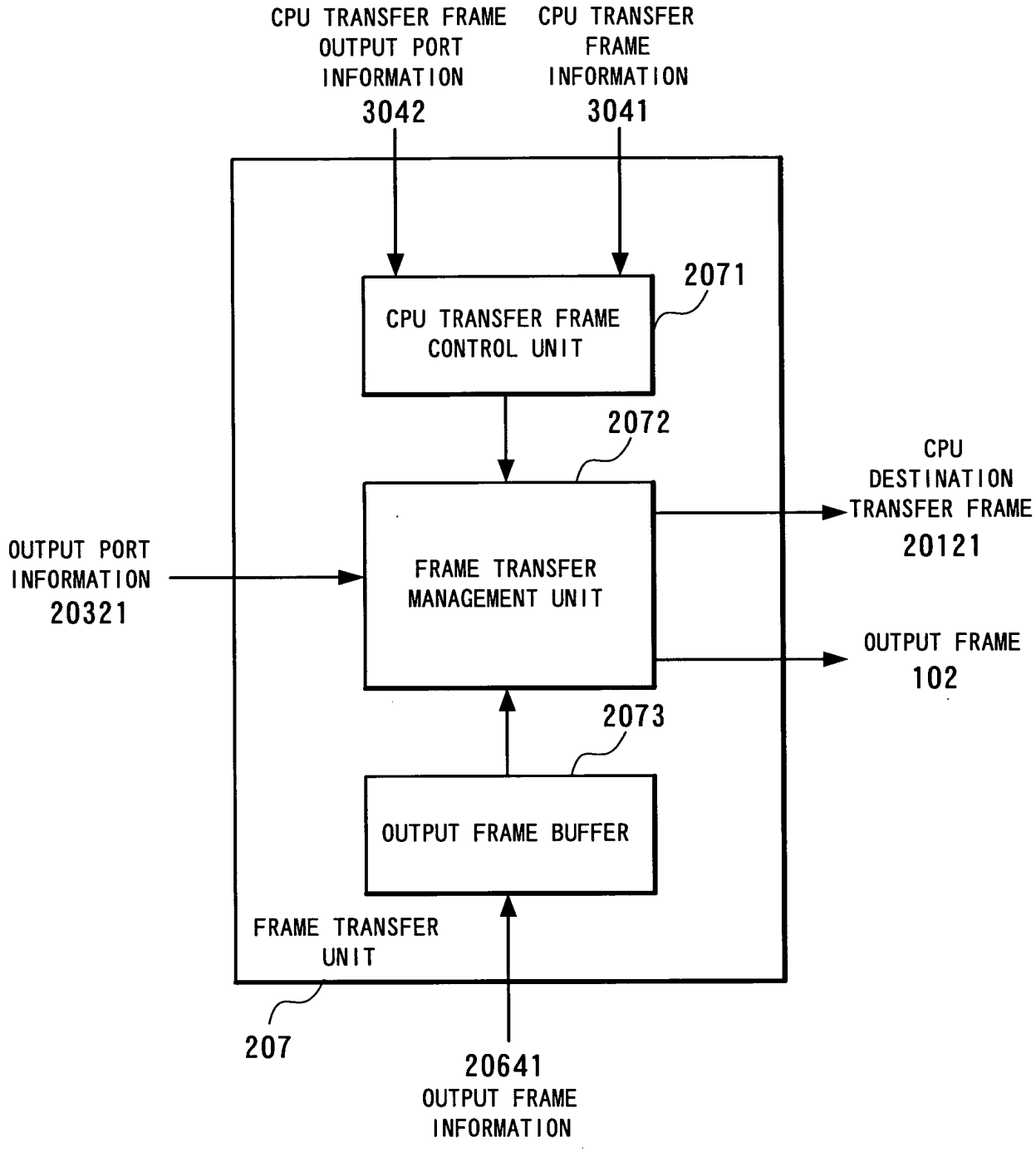

CPU TRANSFER FRAME OUTPUT PORT INFORMATION
3042
CPU TRANSFER FRAME INFORMATION
3041
2071
CPU TRANSFER FRAME CONTROL UNIT
2072
FRAME TRANSFER MANAGEMENT UNIT
OUTPUT PORT INFORMATION
20321
CPU DESTINATION TRANSFER FRAME
20121
OUTPUT FRAME
102
2073
OUTPUT FRAME BUFFER
FRAME TRANSFER UNIT
207
20641
OUTPUT FRAME INFORMATION

FIG 23

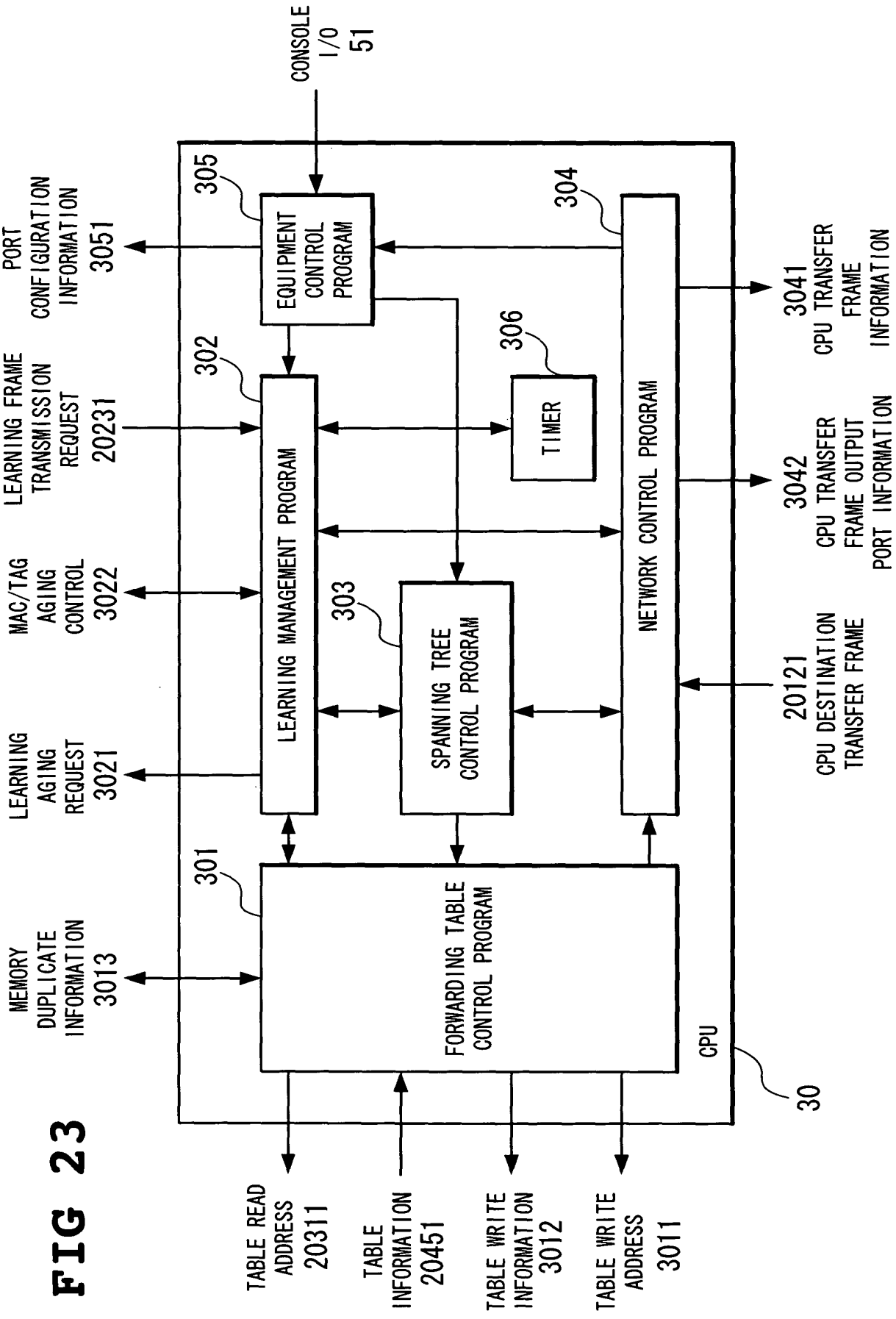

CONSOLE I/O 51
305
EQUIPMENT CONTROL PROGRAM
304
NETWORK CONTROL PROGRAM
PORT CONFIGURATION INFORMATION 3051
3041 CPU TRANSFER FRAME INFORMATION
302
LEARNING MANAGEMENT PROGRAM
306
TIMER
LEARNING FRAME TRANSMISSION REQUEST 20231
3042 CPU TRANSFER FRAME OUTPUT PORT INFORMATION
MAC/TAG AGING CONTROL 3022
303
SPANNING TREE CONTROL PROGRAM
LEARNING AGING REQUEST 3021
20121 CPU DESTINATION TRANSFER FRAME
301
FORWARDING TABLE CONTROL PROGRAM
MEMORY DUPLICATE INFORMATION 3013
CPU
30
TABLE READ ADDRESS 20311
TABLE INFORMATION 20451
TABLE WRITE INFORMATION 3012
TABLE WRITE ADDRESS 3011

FIG.24

70134

DESTINATION FIRST-STAGE TAG INFORMATION	TABLE STORAGE ADDRESS
8100-0000	0x0000, 0x01FF, 0x08EF
8100-0002	0x0300, 0x01DD
⋮	⋮
8100-1000	0x2236, 0x05EA, 0x08BB, 0x31F4
8100-2004	0x21B2
8100-4092	0x78AB, 0x9687
8100-4094	0xF67A

FIG.25

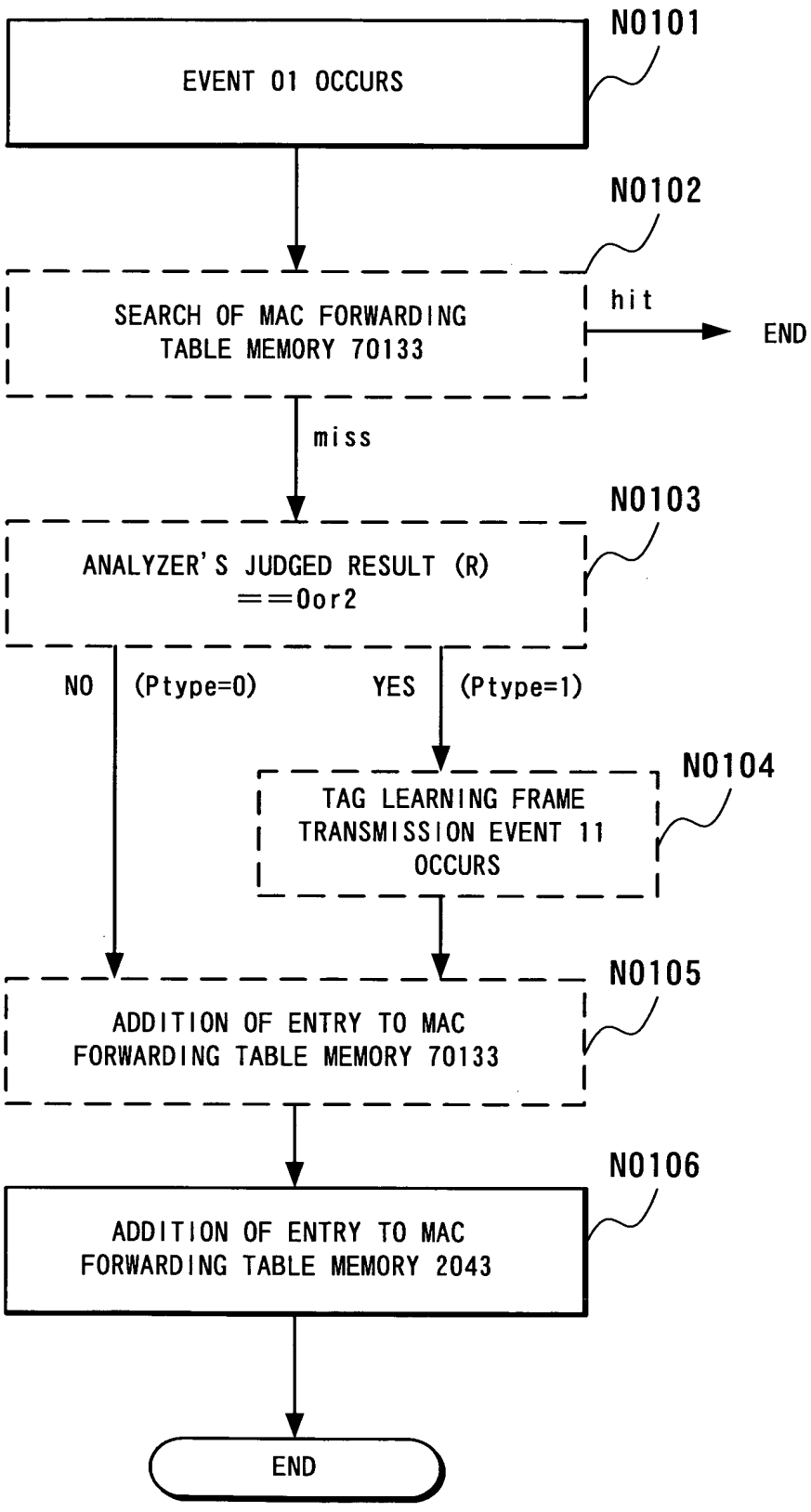

N0101
EVENT 01 OCCURS
N0102
SEARCH OF MAC FORWARDING TABLE MEMORY 70133
hit
END
miss
N0103
ANALYZER'S JUDGED RESULT (R) ==0or2
NO
(Ptype=0)
YES
(Ptype=1)
N0104
TAG LEARNING FRAME TRANSMISSION EVENT 11 OCCURS
N0105
ADDITION OF ENTRY TO MAC FORWARDING TABLE MEMORY 70133
N0106
ADDITION OF ENTRY TO MAC FORWARDING TABLE MEMORY 2043
END

FIG.26

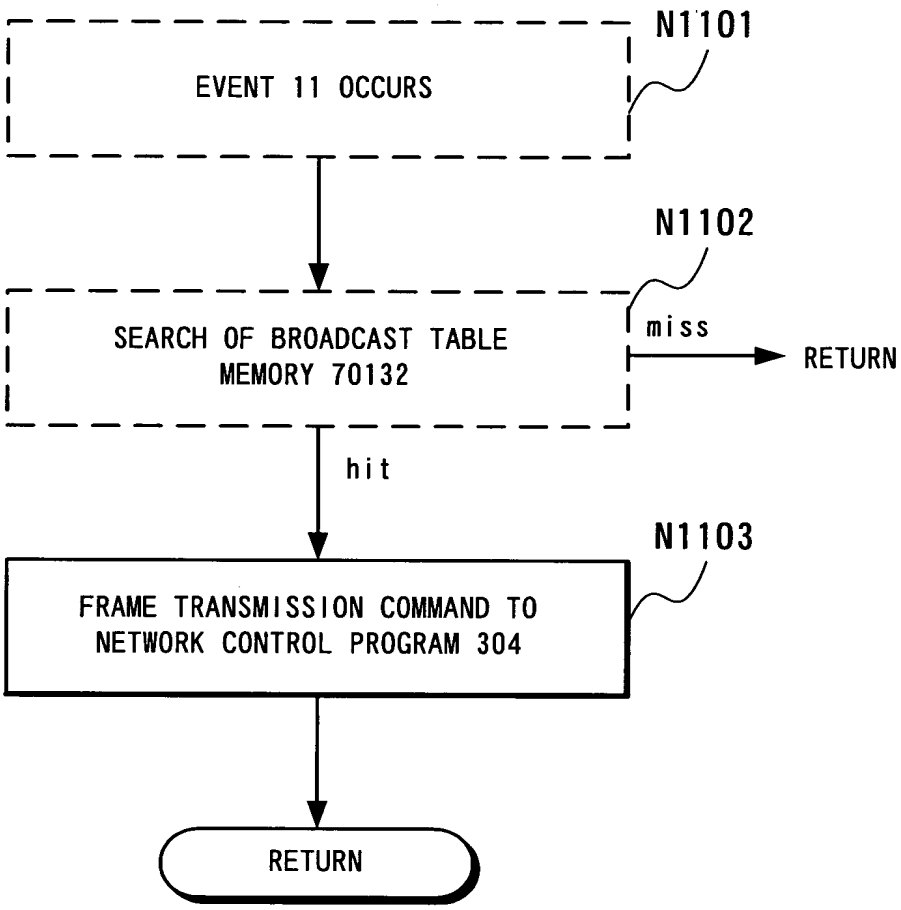

N1101
EVENT 11 OCCURS
N1102
SEARCH OF BROADCAST TABLE MEMORY 70132
miss
RETURN
hit
N1103
FRAME TRANSMISSION COMMAND TO NETWORK CONTROL PROGRAM 304
RETURN

FIG.27

MAC DA&TAG → TAG SETTING (TAG LEARNING)

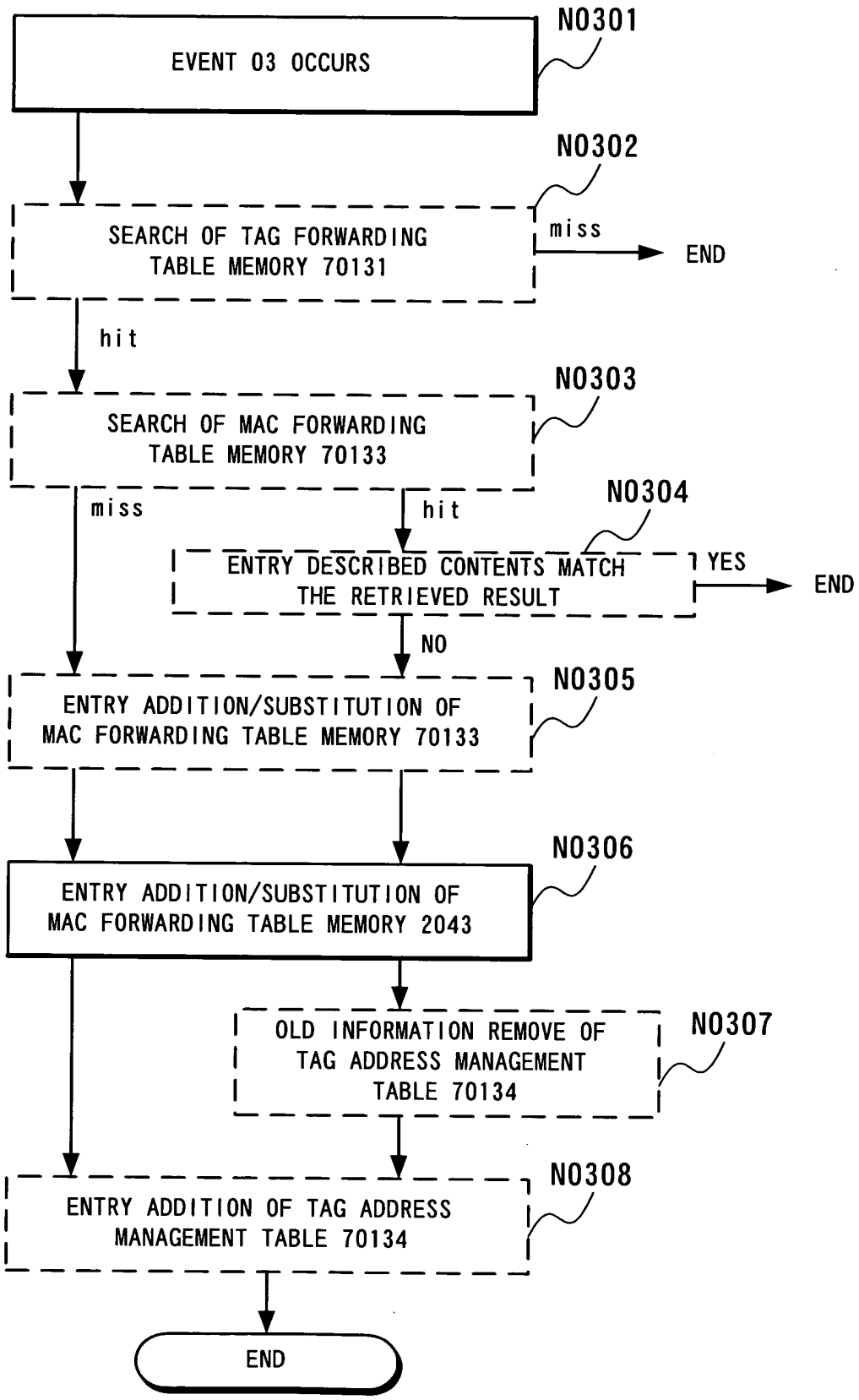


FIG.28

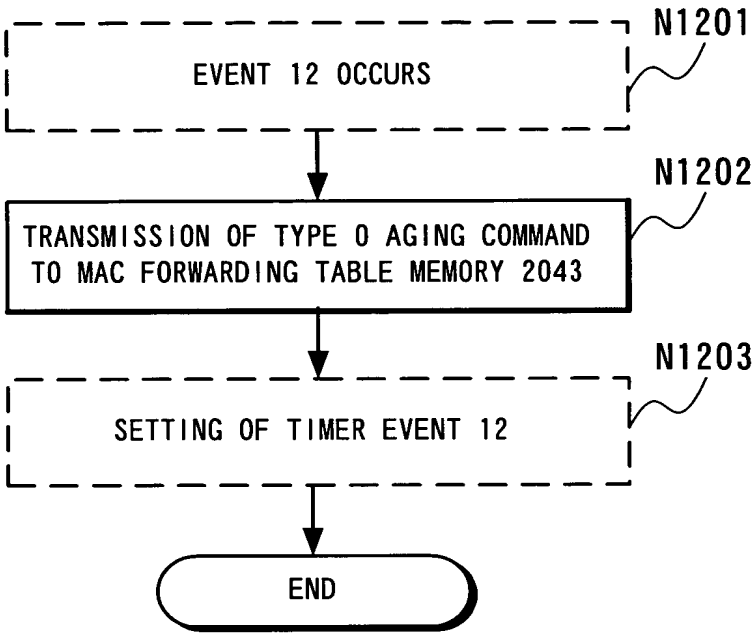

N1201
EVENT 12 OCCURS
N1202
TRANSMISSION OF TYPE 0 AGING COMMAND TO MAC FORWARDING TABLE MEMORY 2043
N1203
SETTING OF TIMER EVENT 12
END

FIG.29

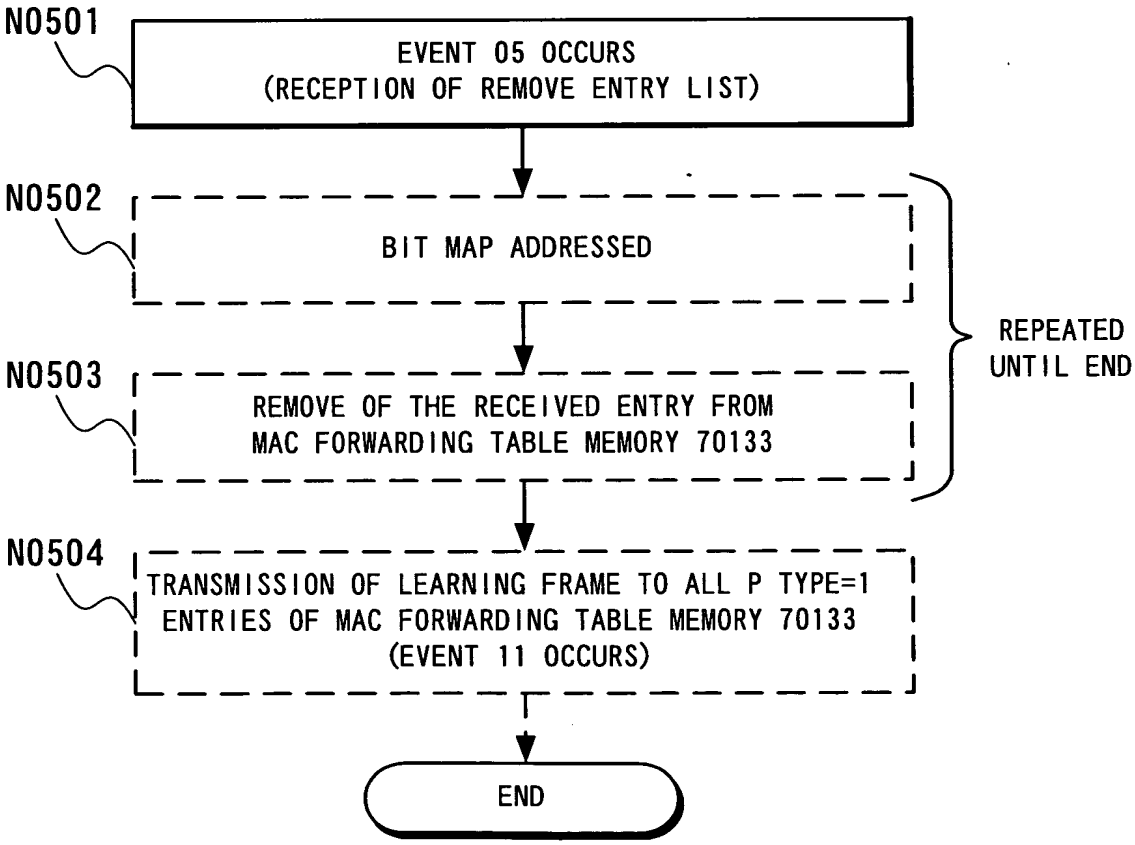

N0501
EVENT 05 OCCURS (RECEPTION OF REMOVE ENTRY LIST)
N0502
BIT MAP ADDRESSED
N0503
REMOVE OF THE RECEIVED ENTRY FROM MAC FORWARDING TABLE MEMORY 70133
REPEATED UNTIL END
N0504
TRANSMISSION OF LEARNING FRAME TO ALL P TYPE=1 ENTRIES OF MAC FORWARDING TABLE MEMORY 70133 (EVENT 11 OCCURS)
END

FIG.30

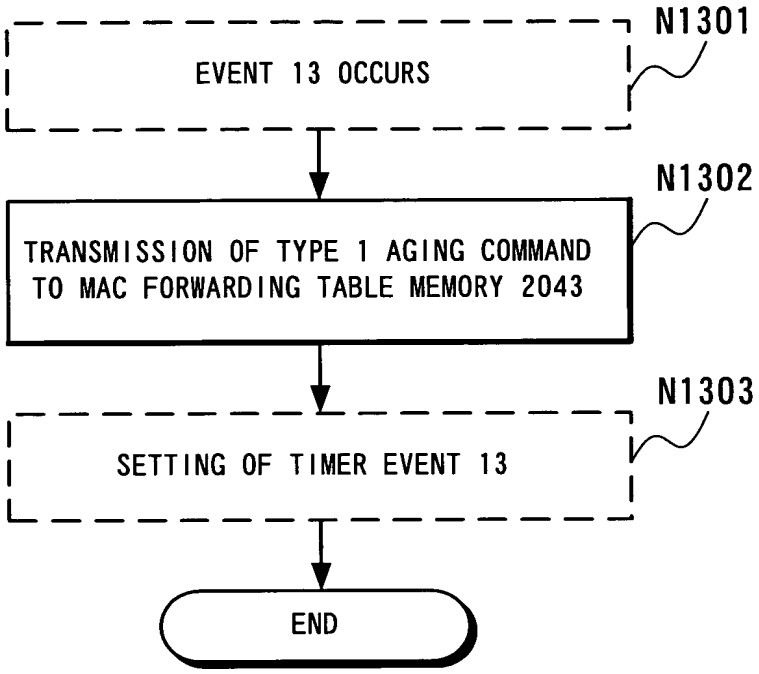

N1301
EVENT 13 OCCURS
N1302
TRANSMISSION OF TYPE 1 AGING COMMAND TO MAC FORWARDING TABLE MEMORY 2043
N1303
SETTING OF TIMER EVENT 13
END

FIG.31

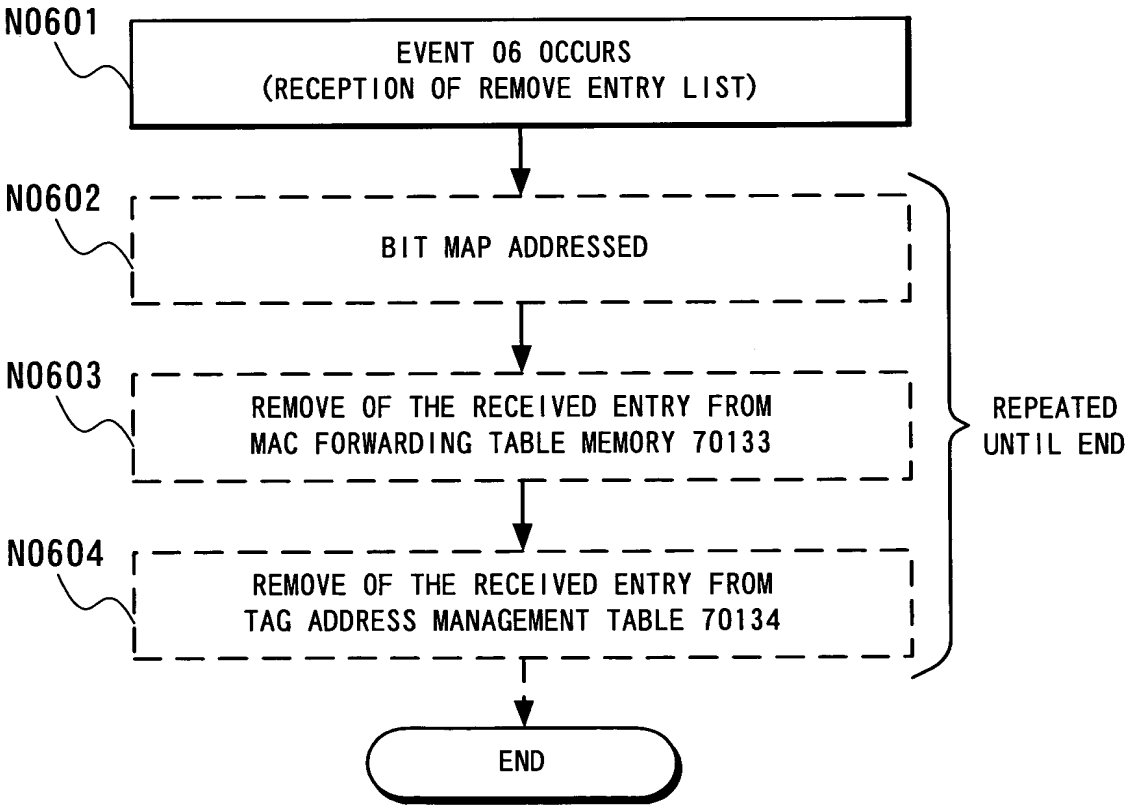

N0601
EVENT 06 OCCURS (RECEPTION OF REMOVE ENTRY LIST)
N0602
BIT MAP ADDRESSED
N0603
REMOVE OF THE RECEIVED ENTRY FROM MAC FORWARDING TABLE MEMORY 70133
N0604
REMOVE OF THE RECEIVED ENTRY FROM TAG ADDRESS MANAGEMENT TABLE 70134
REPEATED UNTIL END
END

FIG 32

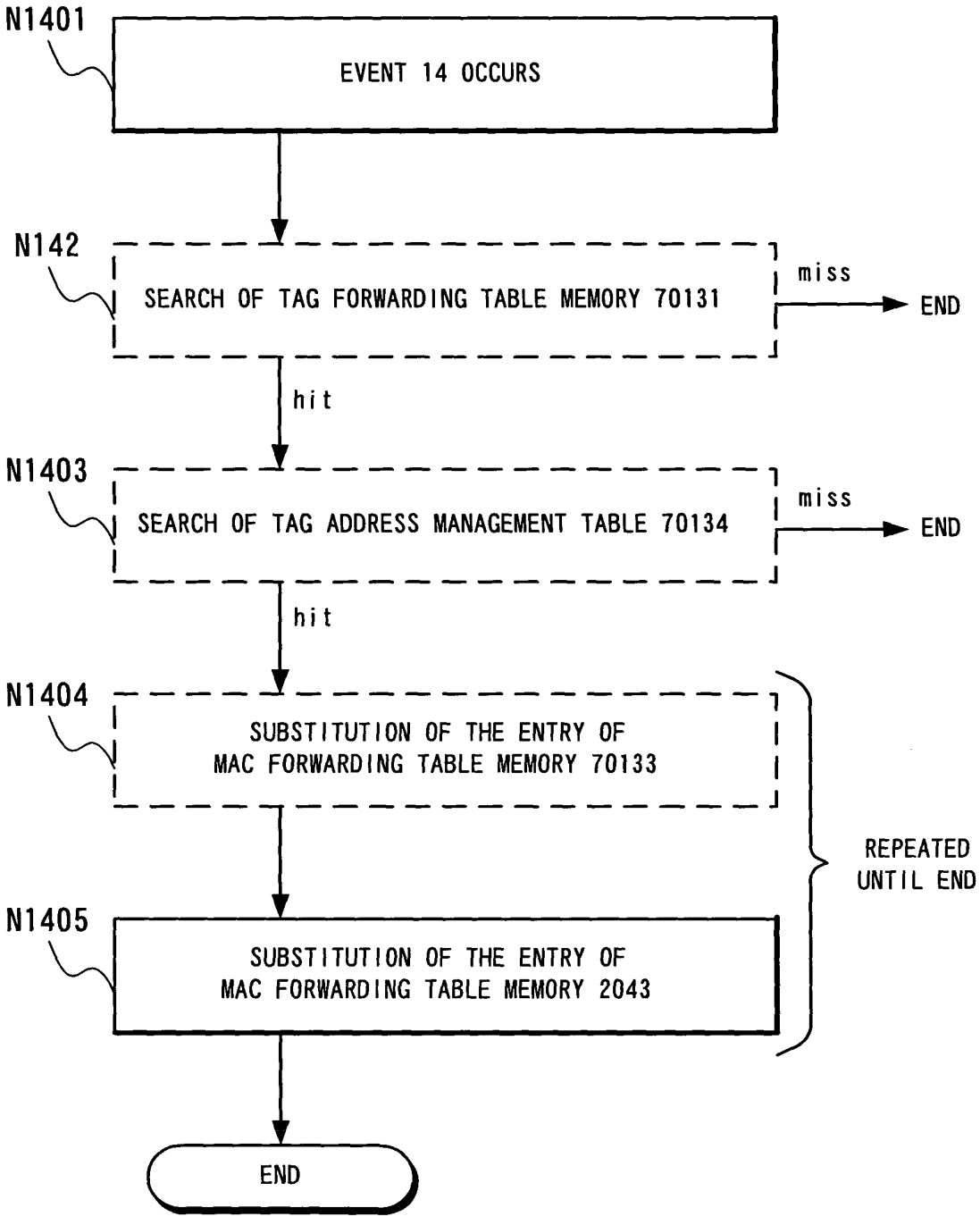

N1401
EVENT 14 OCCURS
N142
SEARCH OF TAG FORWARDING TABLE MEMORY 70131
miss
END
hit
N1403
SEARCH OF TAG ADDRESS MANAGEMENT TABLE 70134
miss
END
hit
N1404
SUBSTITUTION OF THE ENTRY OF
MAC FORWARDING TABLE MEMORY 70133
REPEATED
UNTIL END
N1405
SUBSTITUTION OF THE ENTRY OF
MAC FORWARDING TABLE MEMORY 2043
END

FIG.33

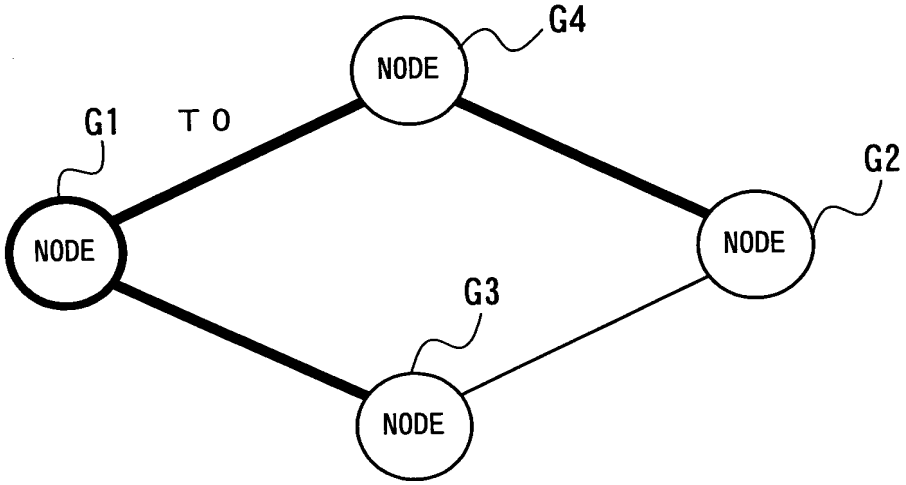


FIG.34

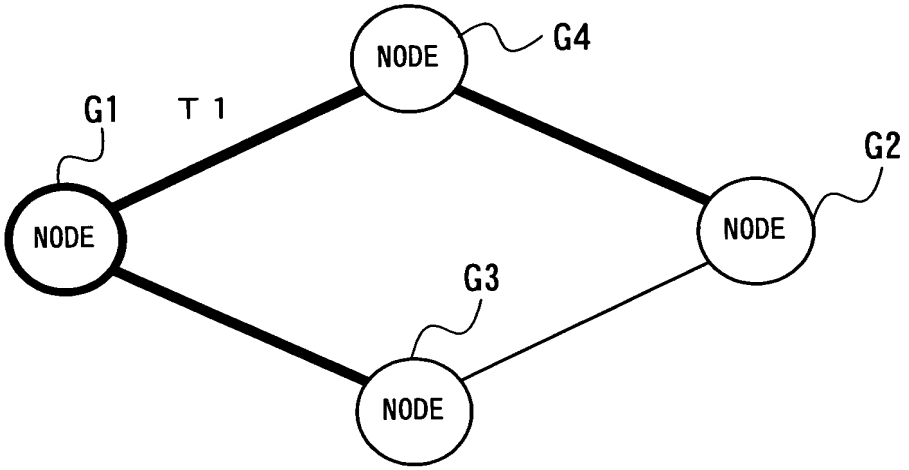


FIG.35

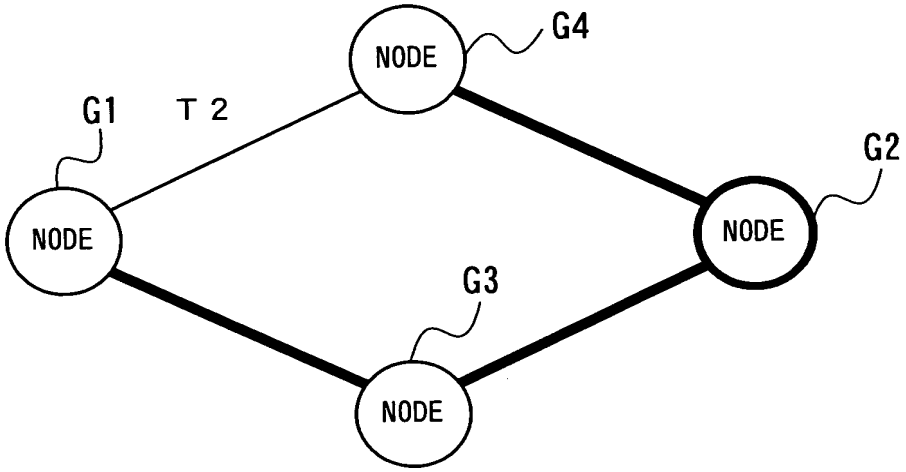


FIG 36

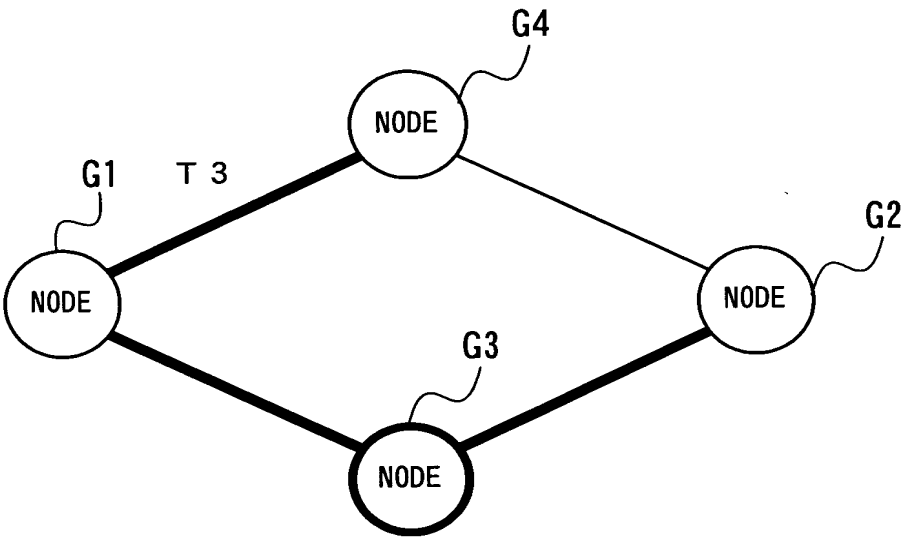

G4
NODE
G1
T 3
G2
NODE
NODE
G3
NODE

FIG.37

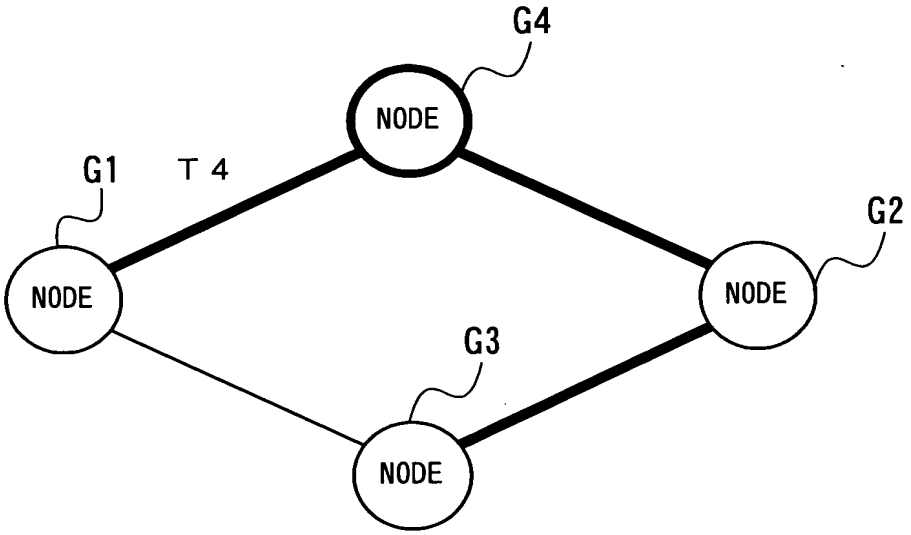

G4
NODE
G1
T 4
G2
NODE
NODE
G3
NODE

FIG.38

EXAMPLE 1: C1→C2 (SAME OPERATION EVEN WHEN G4 IS A CORE. SAME OPERATION EVEN WHEN G3 IS AN EXISTING NODE.)

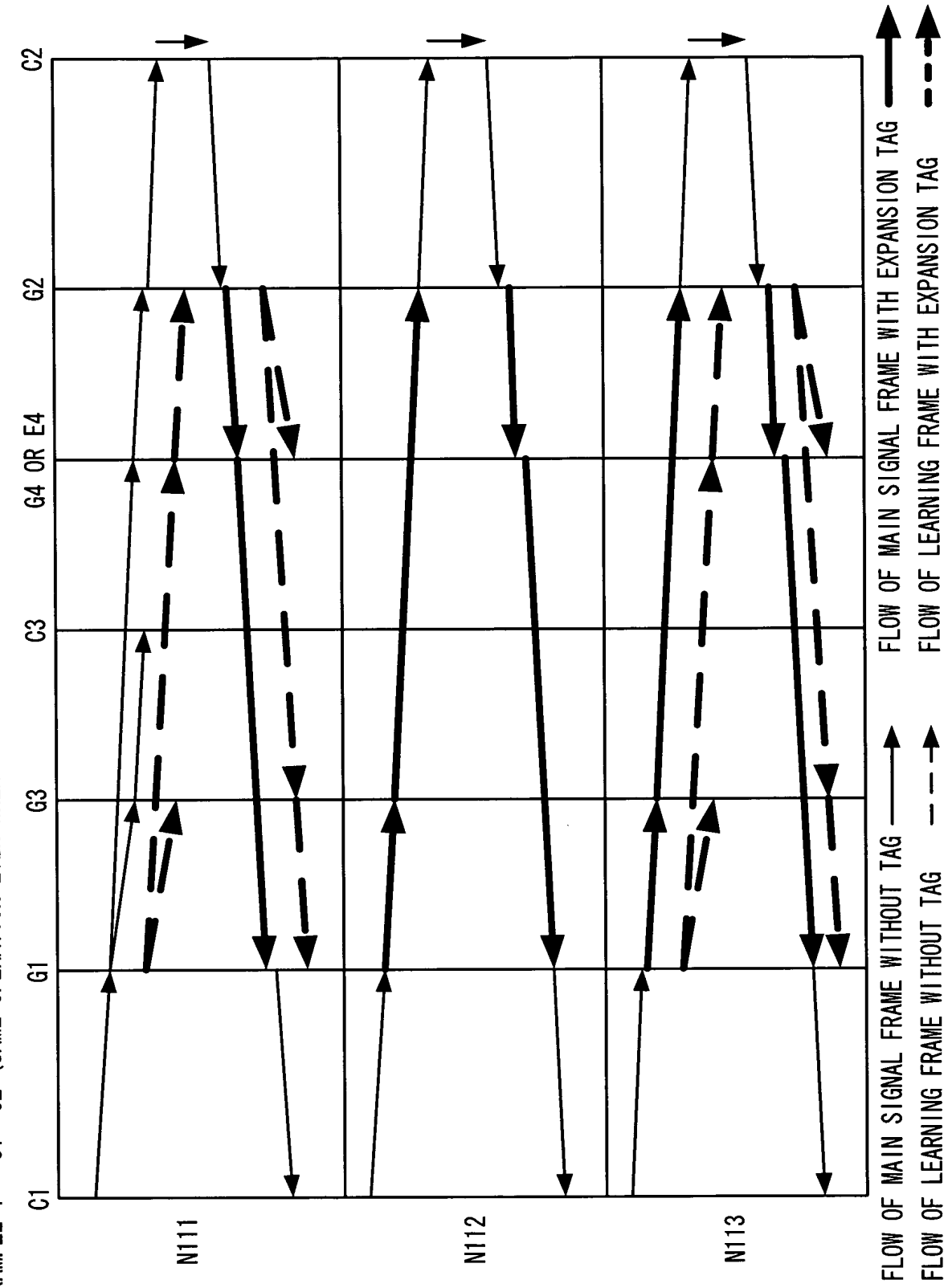


FIG.39

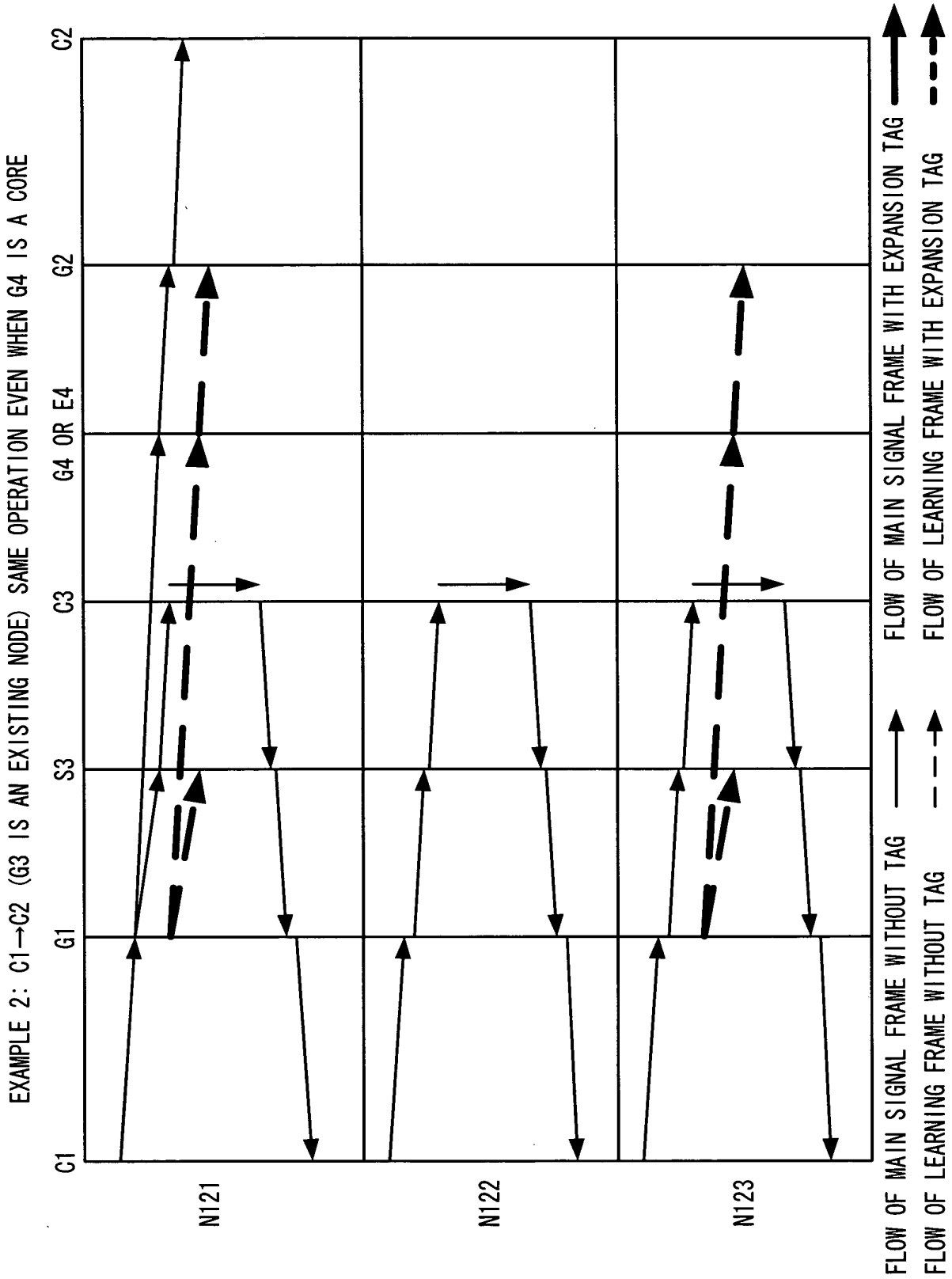
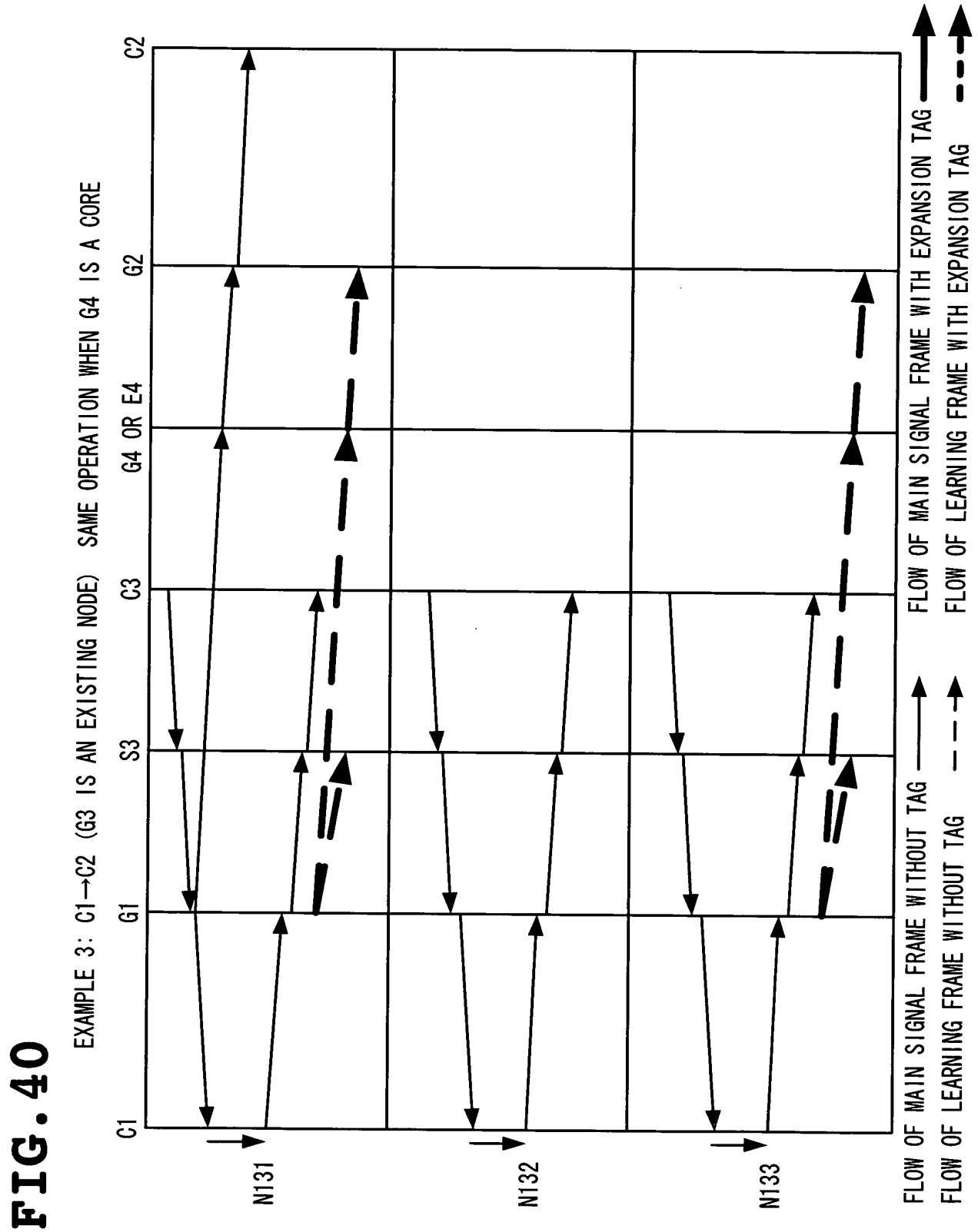

EXAMPLE 2: C1→C2 (G3 IS AN EXISTING NODE) SAME OPERATION EVEN WHEN G4 IS A CORE
C1
G1
S3
C3
G4 OR E4
G2
C2
N121
N122
N123
FLOW OF MAIN SIGNAL FRAME WITHOUT TAG
FLOW OF MAIN SIGNAL FRAME WITH EXPANSION TAG
FLOW OF LEARNING FRAME WITHOUT TAG
FLOW OF LEARNING FRAME WITH EXPANSION TAG

FIG. 40


EXAMPLE 3: C1→C2 (G3 IS AN EXISTING NODE) SAME OPERATION WHEN G4 IS A CORE
C1
G1
S3
C3
G4 OR E4
G2
C2
N131
N132
N133
FLOW OF MAIN SIGNAL FRAME WITHOUT TAG
FLOW OF LEARNING FRAME WITHOUT TAG
FLOW OF MAIN SIGNAL FRAME WITH EXPANSION TAG
FLOW OF LEARNING FRAME WITH EXPANSION TAG